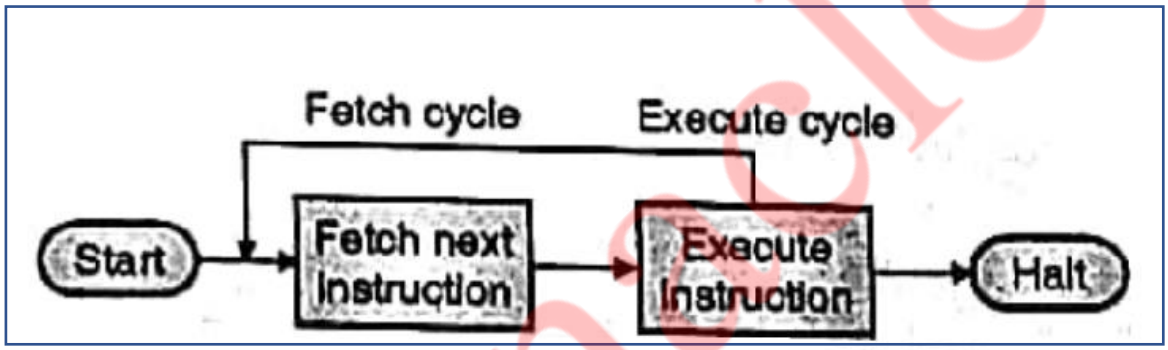
COMPUTER ORGANISATION AND ARCHITECTURE (MAY 2019)

Q.1) Write the following **(20 M)**

a) Explain Instruction and instruction cycle. **(5 M)**

Ans:

- The instruction cycle is a representation of the states that the computer or the microprocessor performs when executing an instruction.
- The instruction cycle comprises of two main steps to be followed to execute the instruction namely the fetch operation in the fetch cycle and the execution operation during the execute cycle.



- It comprises of the fetch cycle and executes cycle in a loop to execute huge number of instructions, until it reaches the halt instruction.
- The fetch cycle comprises of the following operations:
  - Program centre holds address of next instruction to fetch; hence the CPU fetches instruction from memory pointed to by PC. This is done by providing the value of PC to the MAR and giving the Read control signal to the memory. On this memory provides the value in the given address.
  - The PC values has to be incremented to point to the next instruction.
  - The instruction is loaded into Instruction Register from the MBR.
  - Finally the processor interprets or decodes the instruction. The processor performs required operations in execute cycle.
- In the execute cycle the operation asked to be performed by the instruction is done. It may comprise of one or more of the following:
  - Transfer of data between processor and memory or between processor or IO module.
  - Processing of data like some arithmetic or logical operation of data.]
  - Change the sequence of operation i.e. branching instructions.

b) Differentiate between Memory based IO and IO mapped IO. (5 M)

Ans:

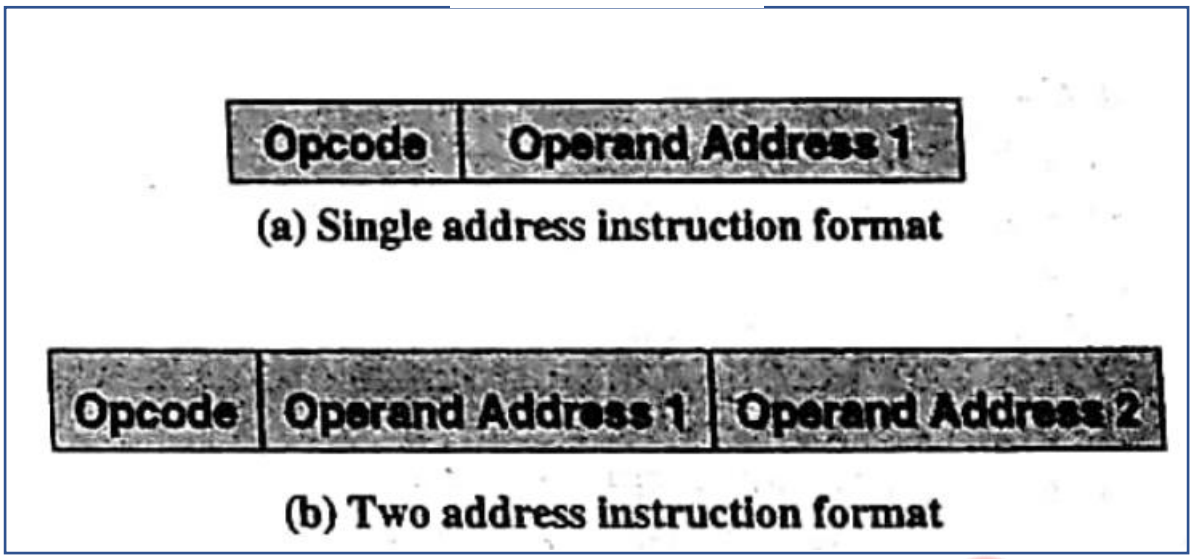
Memory Mapped IO	IO Mapped IO
A method to perform IO operations between the CPU and peripheral devices in a computer that uses one address space for memory and IO devices.	A method to perform IO operations between the CPU and peripheral devices in a computer that uses two separate address spaces for memory and IO device.
Uses the same address space for both memory and IO devices.	Uses two separate address space for memory and IO device
As the memory mapped IO uses one address space for both IO and memory, the available addresses for memory are minimum.	All the addresses can be used by the memory.
Uses the same instructions for both IO and memory operations.	Uses separate instructions for read and write operations in IO and memory.
Less efficient	More Efficient.

---

c) Give different instruction formats. (5 M)

Ans:

- Input devices are required to give the instructions and data to the system. The output devices are used to give the output devices.
- The instructions and data given by the input device are to be stored, and for storage we require memory.
- Elements of Single, two and three address instructions are as follows:
  - Operation code is that part of the instruction which gives the code for the operation to be performed.
  - Source operand reference or address 1, gives the reference of the data on which the operation is to be performed. This address could be a register, memory or an input device.
  - Source operand reference or address 2, gives the reference of the second data on which the operation is to be performed. This address could again be a register, memory or an input device.
  - Result operand reference gives the reference where the result after performing operation is to be stored.
  - An instruction may have only one address with the other two fixed, or may have two addresses with one of the source operand address as the result operand address. Hence the instruction can have one, two or three addresses.



d) Explain memory interleaving Techniques. (5 M)

Ans:

- Interleaved memory implements the concept of accessing more words in single memory access cycle. Memory can be partitioned into N separate memory modules. Thus N accesses can be carried out to the memory simultaneously.
- Once presented with a memory address, each memory module returns one word per cycle. It is possible to present different addresses to different memory modules so that parallel access to multiple words can be done simultaneously or in pipelined fashion.
- The maximum processor bandwidth in interleaved memory can be equal to the number of modules i.e. N words per cycle.
- To achieve the address interleaving consecutive addresses are distributed among the N interleaved modules.
- Interleaving spreads contiguous memory locations across m modules horizontally. This implies that the low-order a bits of the memory address are used to identify the memory module.
- The high order b bits are used to address a word inside a module. Same word address is applied to all memory modules simultaneously. A module address decoder is used to distribute module addresses.\access of the m modules can be overlapped in a pipelined fashion. For this purpose, the memory cycle is subdivided into m sub cycles.

e) Explain superscalar architecture. (5 M)

Ans:

- Superscalar processor are those processors that have multiple execution units.

- Hence these processors can execute the independent instructions simultaneously and hence with the help of this parallelism it increases the speed of the processor.
- It has been that the number of independent consecutive instructions 2 to 5. Hence the instruction issue degree in a superscalar processor is restricted from 2 to 5.

Pipelining in Superscalar Processor:

- The pipelining is the most important representation of demonstrating the speed increase by the superscalar feature of processor.
- Hence to implement multiple operations simultaneously, we need to have multiple execution units to execute each instruction independently.
- The ID and rename unit, decodes the instruction and then by the use of register renaming avoids instruction dependency. The instruction window takes the decoded instructions and based on some pair ability rules, issues them to the respective execution units.
- The instructions once executed move to the Retire and write back unit, wherein the instructions retire and the result is written back to the corresponding destination.

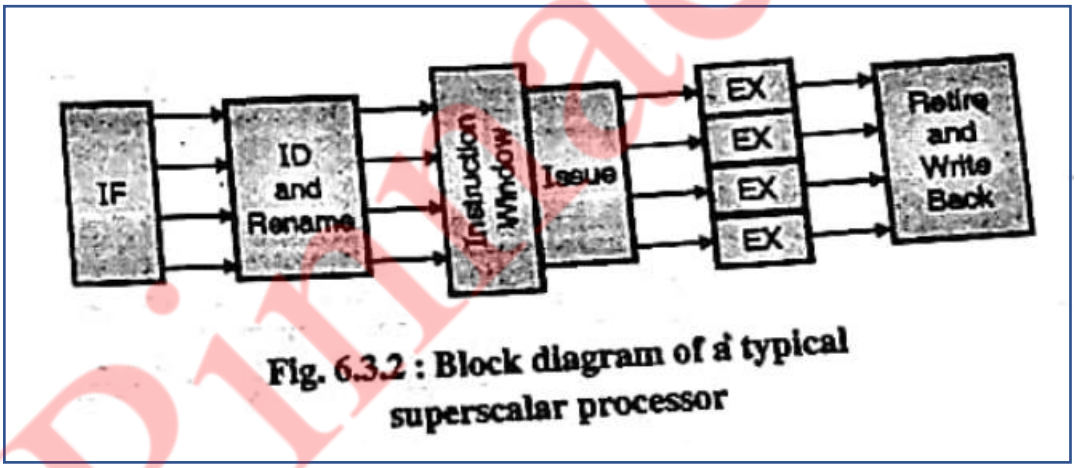
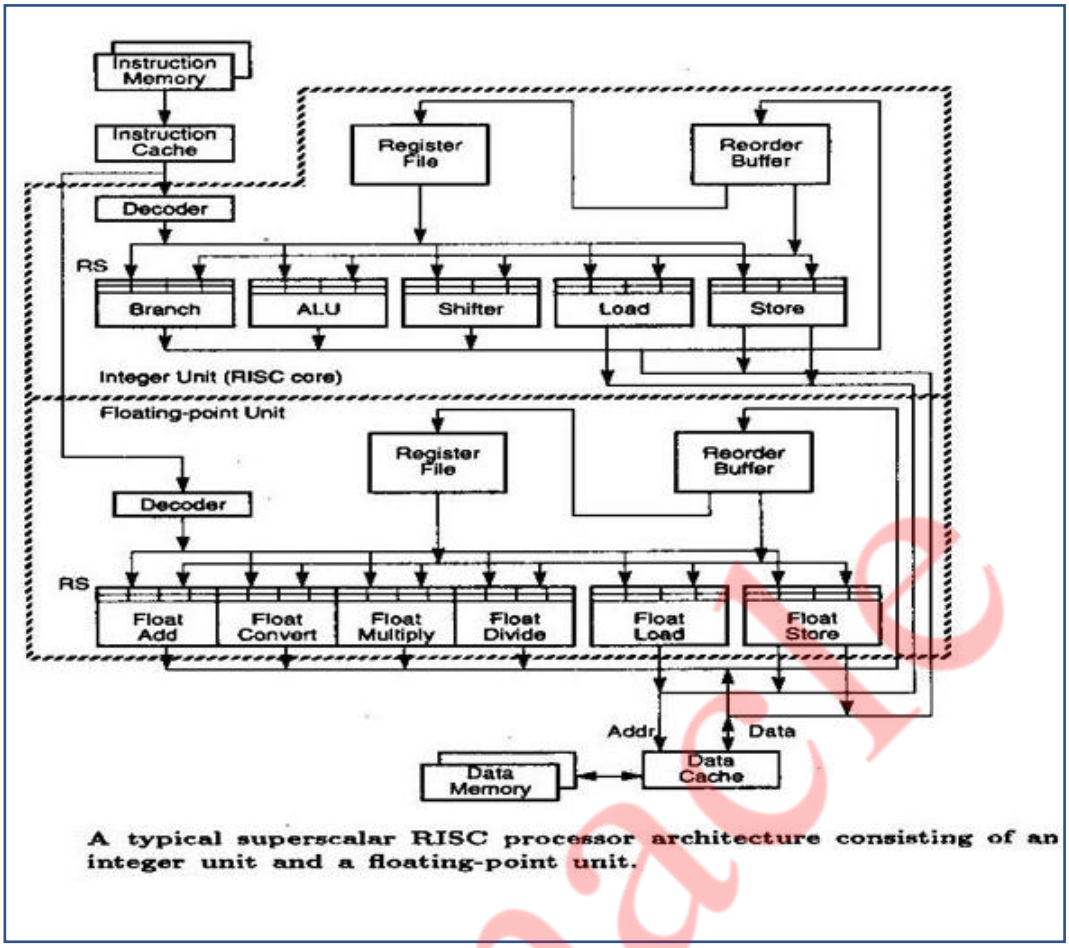


Fig. 6.3.2 : Block diagram of a typical superscalar processor

- A RISC or CISC processors execute one instruction per cycle. Their performance can be improved with superscalar architecture:
  - Multiple instruction pipelines are used.
  - Multiple instructions are issued for execution per cycle.
  - Multiple results are generated per cycles.

- Superscalar processors can exploit more instruction level parallelism in user program.



A typical superscalar RISC processor architecture consisting of an integer unit and a floating-point unit.

Q.2)

a) Explain Branch Prediction Logic and Delayed Branch. (10 M)

Ans:

- Performance gain through pipelining can be reduced by the presence of program transfer instructions (such as JMP, CALL, RET and conditional jumps).
- They change the sequence causing all the instructions that entered the pipeline after program transfer instruction invalid.
- Suppose instruction I3 is a conditional jump to I50 at some other address (target address), then the instructions that entered after I3 is invalid and new sequence beginning with I50 need to be loaded in.
- This causes bubbles in pipeline, where no work is done as the pipeline stages are reloaded.
- To avoid this problem, the Pentium uses a scheme called Dynamic Branch Prediction.
- In this scheme, a prediction is made concerning the branch instruction currently in pipeline.
- Prediction will be either taken or not taken.

- If the prediction turns out to be true, the pipeline will not be flushed and no clock cycles will be lost. If the prediction turns out to be false, the pipeline is flushed and started over with the correct instruction.
- It results in a 3 cycle penalty if the branch is executed in the u-pipeline and 4 cycle penalty in v-pipeline.
- It is implemented using a 4-way set associative cache with 256 entries. This is referred to as the Branch Target Buffer (BTB).
- The directory entry for each line contains the following information:
- Valid Bit : Indicates whether or not the entry is in use.
- History Bits: track how often the branch has been taken.
- Source memory address that the branch instruction was fetched from (address of I3).
- If its directory entry is valid, the target address of the branch is stored in corresponding data entry in BTB.

Delayed Branch:

- Compiler detects branch instruction and rearranges the machine language code sequence by inserting useful instructions and rearranges the code sequence to reduce the delays incurred by Branch Instruction.

---

b) A program having 10 instructions (without Branch and Call Instructions) is executed on non-pipeline and pipeline processors. All instructions are of same length and having 4 pipeline stages and time required to each stage is 1nsecc.

I. Calculate time required to execute the program or Non-pipeline and Pipeline processor.

II. Calculate Speedup. (10 M)

Ans:

I. Given: n = 10 instructions, K = 4, t = 1nsec

Execution time pipelined = (4 + 100 - 1) * t

= (4 + 90) * 1

= 94 nsec.

Execution time unpipelined = (K * t) n

= (4 * 1) 1

= 4 nsec.

II. Speedup = 4/94 **= 0.043 times.**

Q.3)

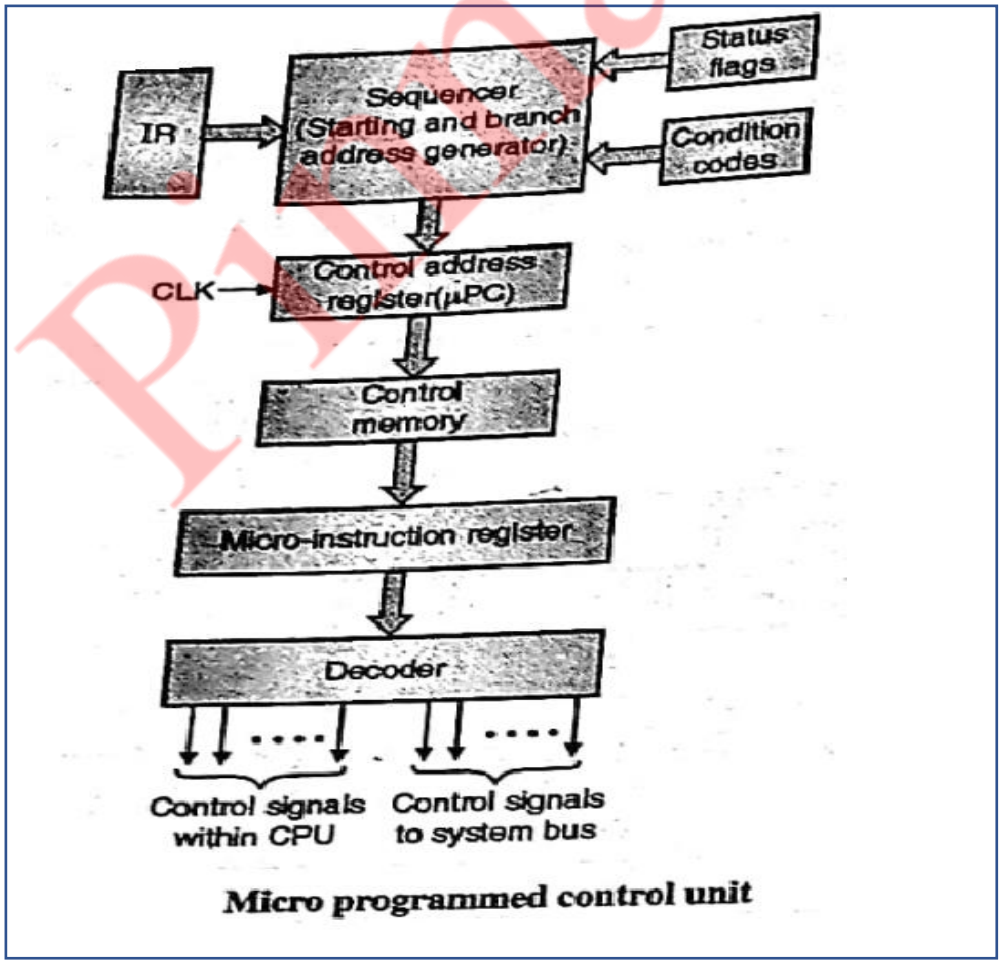
a) Explain different technique for design of control unit of computer.

(10 M)

Ans:

Micro Programmed Control unit:

- Micro programmed control unit generates control signals based on the microinstructions stored in a special memory called as the control memory.
- Each instruction points to a corresponding location in the control memory that loads the control signals in the control register.
- The control register is then read by a sequencing logic that issues the control signals in a proper sequence.
- The implementation of the micro programmed.
- The instruction register (IR), status flag and condition codes are read by the sequencer that generates the address of the control memory location for the corresponding instruction in the IR.
- This address is stored in the control address register that selects one of the locations in the control memory having the corresponding control signals.
- These control signals are given to the microinstruction register, decoded and then given to the individual components of the processor and the external devices.



Micro programmed control unit

Wilkie's Microprogrammed(Hard Wired) Control Unit:

- First working model of micro-programmed control unit was proposed by Wilkies in 1952. In above design, a microinstruction has two major components:
  - Control field
  - Address field
- The control memory access register can be loaded from an external source as well as from the address field of microinstructions. A machine instruction typically provides the starting address of a micro-program in control memory.
- On the basis of starting address from instruction register, decoder activates one of the eight output lines.
- This activated lines, in turn generates control signals and the address of the next microinstruction to be executed.
- This address is once again fed to the CMAR resulting in activation of another control line and address field.
- This process is repeated till the execution of the instruction is achieved.

---

b) What is micro program? Write microprogram for following operations

I. ADD R1, M, Register R1 and Memory location M are added and result store at Register R1.

II. MUL R1, R2 Register R1 and Register R2 are multiplied and result store at Register R1. (10 M)

Ans:

- Microprogramming is a process of writing microcode for a microprocessor. Microcode is low-level code that defines how a microprocessor should function when it executes machine-language instructions.
- Typically, one machine language instruction translates into several microcode instruction, on some computers, the microcode is stored in ROM and cannot be modified.
- **Micro Program to add R1, M.**

T-state	Operation	Microinstructions
T 1	PC → MAR	PCout, Marin, Read, Clear y, set Cin, Add, Zinn
T 2	M → MBR PC ← PC + 1	Zout, PCin, Wait for memory fetch cycle
T 3	MBR → IR	MBRout, IRin
T 4	R1 → x	R1out, Xin, CLRC
T 5	M → ALU	Mout, ADD, Zin
T 6	Z → R1	Zout, R1in

T 7	Check for intr	Assumption enabled intr pending, CLRX, SETC, Spout, SUB, Zin
T 8	SP ← SP – 1	Zout, Spin, MARin
T 9	PC → MDR	PCout, MDRin, WRITE
T 10	MDR → [SP]	Wait for Mem access
T11	PC ← IS Raddr	PCin IS Raddr out.

- **Micro Program to MUL R1, R2**

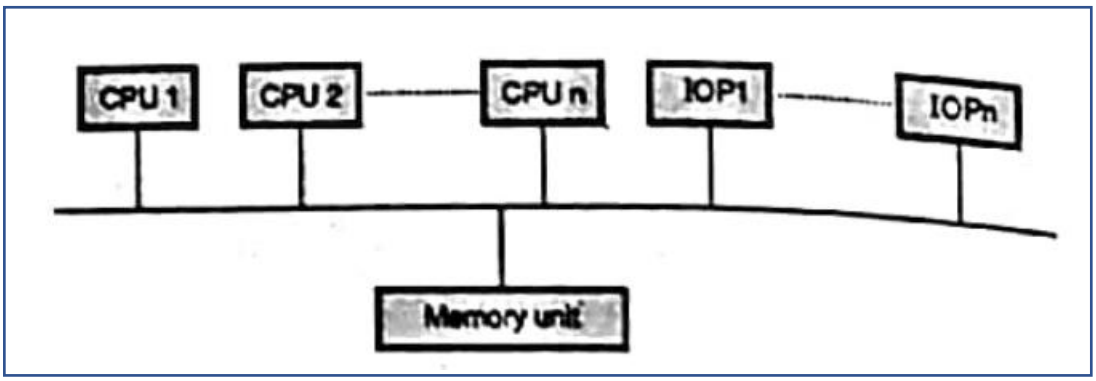
T-state	Operation	Microinstructions
T 1	PC → MAR	PCout, Marin, Read, Clear y, set Cin, Add, Zinn
T 2	M → MBR PC ← PC + 1	Zout, PCin, Wait for memory fetch cycle
T 3	MBR → IR	MBRout, IRin
T 4	R1 → x	R1out, Xin, CLRC
T 5	R2 → ALU	R2out, MUL, Zin
T 6	Z → R1	Zout, R1in
T 7	Check for intr	Assumption enabled intr pending, CLRX, SETC, Spout, SUB, Zin
T 8	SP ← SP – 1	Zout, Spin, MARin
T 9	PC → MDR	PCout, MDRin, WRITE
T 10	MDR → [SP]	Wait for Mem access
T11	PC ← IS Raddr	PCin IS Raddr out.

Q.4)

a) Explain Bus Contention and different method to resolve it. (10 M)

Ans:

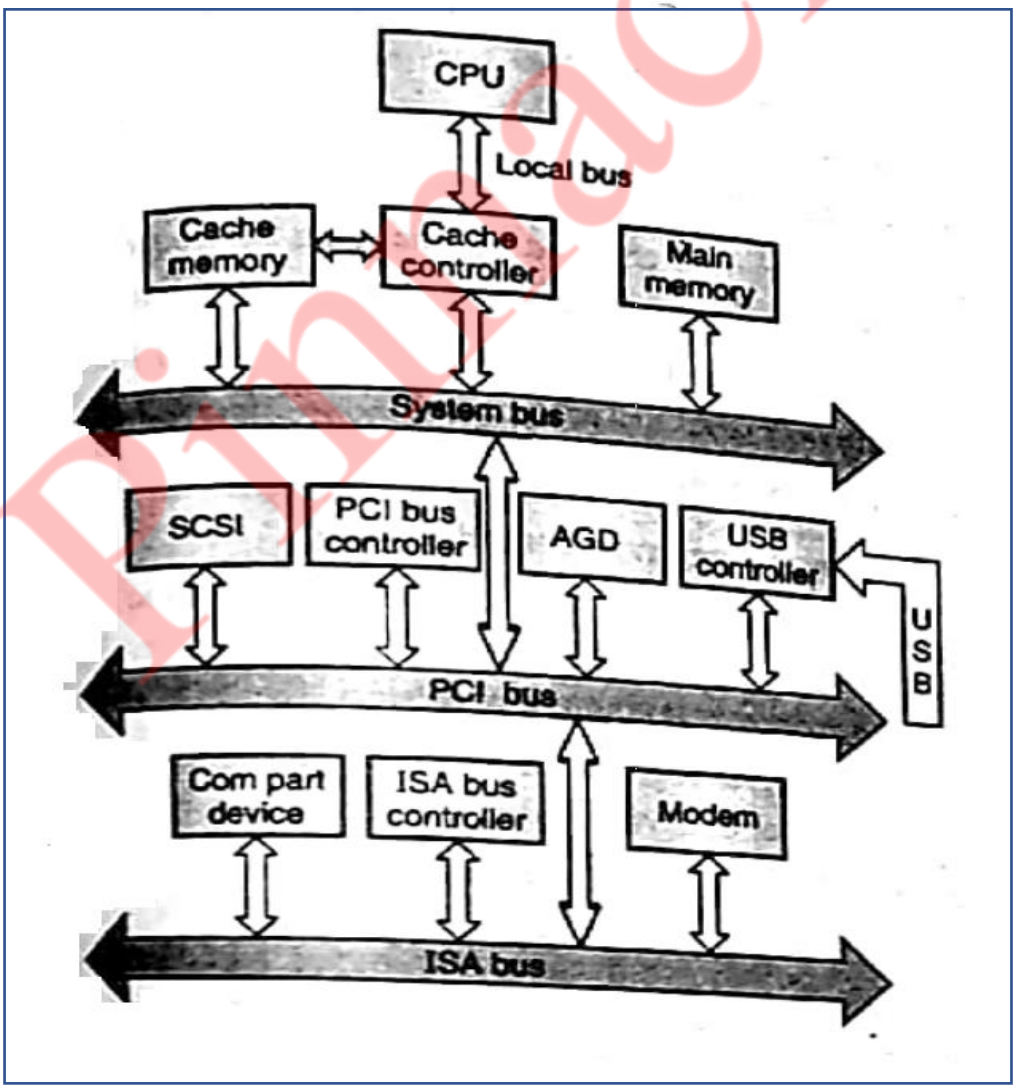
- In a bus system, processors, memory modules and peripheral devices are attached to the bus. The bus can handle only one transaction at a time between a master and slave. In case of multiple requests, the bus arbitration logic must be able to allocate or deallocate and it should service request at a time.
- Thus, such a bus is a time sharing or contention bus among multiple functional modules. As only one transfer can take place at any time on the bus, the overall performance of the system is limited by the bandwidth of the bus.
- When number of processors contending to acquire a bus exceeds the limit then a single bus architecture may become a major bottleneck. This may cause a serious delay in servicing a transaction.



- Aggregate data transfer demand should never exceed the capacity of the bus. This problem can be countered to some extent by increasing the data rate of the bus and by using a wider bus.
- Method of avoiding contention is multiple bus hierarchy.

Multiple-Bus Architecture:

- If a greater number of devices are connected to the bus, performance will suffer due to following reasons:



- In general, the more devices attached to the bus, the greater will be propagation delay.
- The bus may become a bottleneck as the aggregate data transfer demand approaches the capacity of the bus.
- This problem can be countered to some extent by increasing the data rate the bus can carry and by using wider buses.
- Most computer systems enjoy the use of multiple buses. These buses are arranged in a hierarchy.

---

b) Explain Different data transfer Technique. (10 M)

Ans:

Programmed I/O

- In the programmed I/O method of interfacing. CPU has direct control over I/O.
- The processor checks the status of the devices and issues read or write commands and then transfer data. During the data transfer. CPU waits for I/O module to complete operation and hence this system wastes the CPU time.
- The sequence of operations to be carried out in programmed I/O operation are:
  - CPU requests for I/O operation.
  - I/O module performs the said operation.
  - I/O module update the status bits.
  - CPU checks these status bits periodically. Neither the I/O module can inform CPU directly nor can I/O module interrupt CPU.
  - CPU may wait for the operation to complete or may continue the operation later.

Interrupt driven I/O

- Interrupt driven I/O overcomes the disadvantage of programmed I/O i.e. the CPU waiting for I/O device.
- This disadvantage is overcome by CPU not repeatedly checking for the device being ready or not instead the I/O module interrupts when ready.
- The sequence of operations for interrupt Driven I/O is as below:
  - CPU issues the read command to I/O device.
  - I/O module gets data from peripheral while CPU does other work.
  - Once the I/O module completes the data transfer from I/O device, it interrupts CPU.
  - On getting the interrupt, CPU requests data from the I/O module.
  - I/O module transfers the data to CPU.
- The interrupt driven I/O mechanism for transferring a block of data.
- After issuing the read command the CPU performs its work, but checks for the interrupt after every instruction cycle.
- When CPU gets an interrupt, it performs the following operation in sequence:

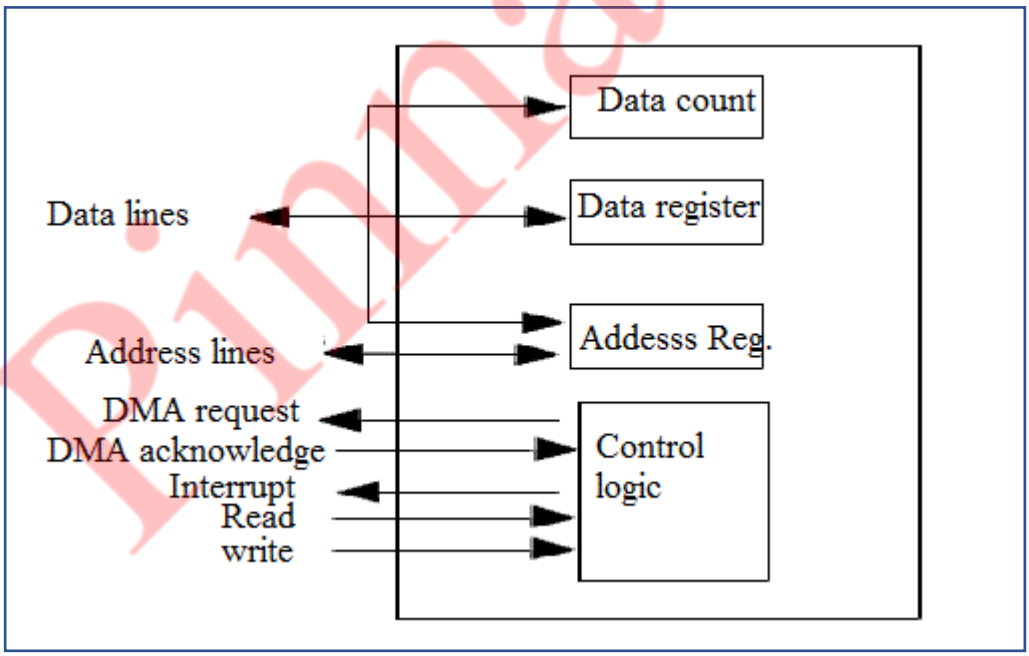
- Save context i.e. the contents of the registers on the stack
- Processes interrupt by executing the corresponding ISR
- Restore the register context from the stack.

Transferring a word of data

- CPU issues a 'READ' command to I/O device and then switches to some other program. CPU may be working on different programs.
- Once the I/O device is ready with the data in its data register. I/O device signals an interrupt to the CPU.
- When then interrupt from I/O device occurs, it suspends execution of the current program, reads from the port and then resumes execution of the suspended program.

Data Transfer Modes

- DMA stands for Direct Memory Access. The I/O can directly access the memory using this method.
- Interrupt driven and programmed I/O require active operation of the CPU. Hence transfer rate is limited and CPU is also busy doing the transfer operation. DMA is the solution to this problem.
- DMA controller takes over the control of the bus form CPU for I/O transfer.



- The address register is used to hold the address of the memory location from which the data is to be transferred. There may be multiple address registers to hold multiple addresses.
- The address may be incremented or decremented after every transfer based on mode of operation.
- The data count register is used to keep a track of the number of bytes to be transferred. The counter register is decremented after every transfer.

- The data register is used in a special case i.e. when the transfer of a block is to be done from one memory location to another memory location.
- The DMA controller is initially programmed by the CPU, for the count of bytes to bee transferred address of the memory block for the data to be transferred etc.
- During this programming DMAC, the read and write lines work as inputs for DMAC.
- Once the DMAC takes the control of the system bus i.e. transfers the data between the memory and I/O device, these read and write signals work as output signals.
- They are used to tell the memory that the DMAC wants to read or write from the memory according to the operation being data transfer from memory to I/O or from I/O to memory.

DMA Transfer Modes:

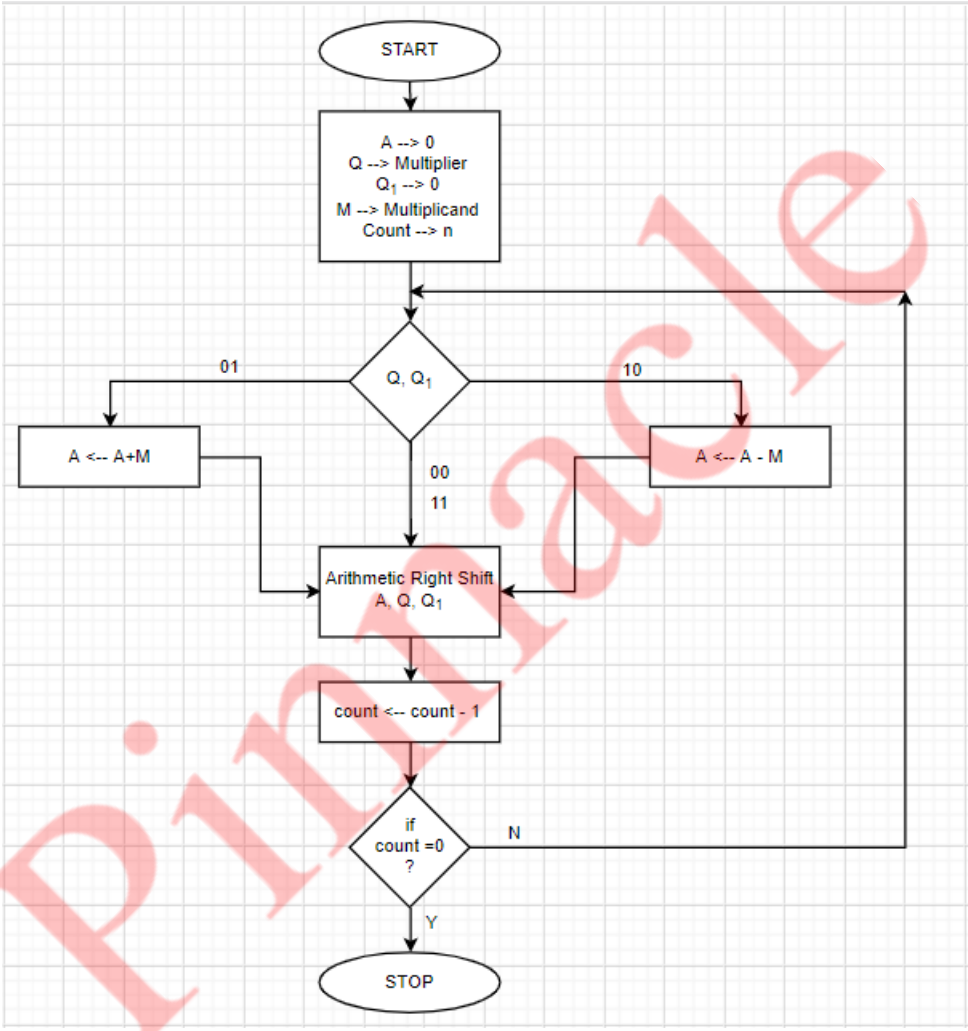
- **Single transfer mode:** In this, the device is programmed to make one byte transfer only after getting the control of system bus.
- After transferring one byte the control of the bus will be returned back to the CPU.
- The word count will be decremented and the address decremented or incremented following each transfer.
- **Block transfer Mode:** In this, the device is activated by DREQ or software request and continues making transfers during the service until a Terminal Count, or an external End of Process is encountered.
- The advantage is that the I/O device gets the transfer of data a very faster speed.
- **Demand Transfer Mode:** In this, the devices continues making transfer until a Terminal Count or external EOP is encountered, or until DREQ goes inactive.
- Thus, transfer may continue until the I/O device has exhausted its data handling capacity.
- **Hidden Transfer Mode:** In this, the DMA controller takes over the charge on the system bus and transfers data when processor does not needs system bus.
- The processor does not even realize of this transfer being taking place.
- Hence these transfer are hidden from the processor.

Q.5)

a) Explain Booth's Multiplication algorithm and Perform $(17)_{10} * (5)_{10}$ (10 M)

Ans:

Booth's principle states that "The value of series of 1's of binary can be given as the weight of the bit preceding the series minus the weight of the last bit in the series."



Given: m = 17 = $(010001)_2$

Q = 5 = $(000101)_2$

-m = $(111010)_2$

A	Q	Q_{-1}	m
000000	000101	0	010001
+111010			
111010	000101	0	

111101	000010	1
+010001		
001110	000010	1
000111	000001	0
+111010		
100001	000001	0
010000	100000	1
+111010	100000	1
011010	100000	1
001101	010000	0
000110	101000	0
000011	010100	0
000001	101010	0
000000	110101	0
000000	101010	1

$(1010101)_2 = (85)_{10}$

b) Consider a cache memory of 16 words. Each block consists of 4 words. Size of the main memory is 256 bytes. Draw associative mapping and calculate TAG, and word size. (10 M)

Ans:

Given:

Cache Memory = 16 words

Block consist of 4 words

Main memory = 256 bytes

Main memory = 256 * 16 words = $2^8 * 2^4 = 2^{12}$

TAG field = 2^{12} = 12 bits consist of both set field and TAG field.

SET + TAG = 12

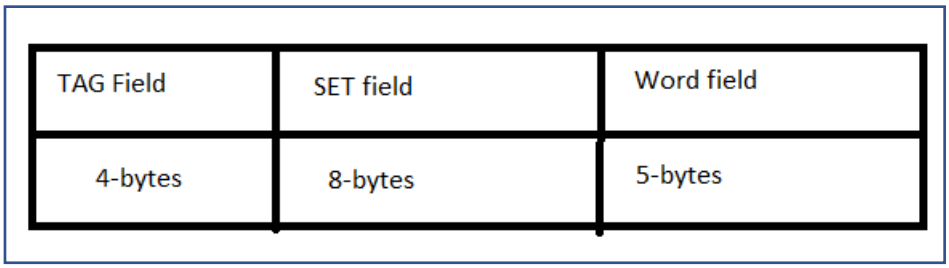
4 + TAG = 12

TAG = 12 – 4

TAG = 8 bytes.

Word size = As there are 8 blocks and each block consist of 4 words,

Hence 8 * 4 = 32 = 2^5



TAG Field	SET field	Word field
4-bytes	8-bytes	5-bytes

Q.6)

a) Explain Different type of pipeline hazards. (10 M)

Ans:

- Instruction hazards occur when instructions read or write registers that are used by other instructions. The type of conflicts are divided into three categories:
  - Structural Hazards (resource conflicts)
  - Data Hazards (Data dependency conflicts)
  - Branch difficulties (Control Hazards)
- **Structural hazards:** these hazards are caused by access to memory by two instructions at the same time. These conflicts can be slightly resolved by using separate instruction and data memories.
- It occurs when the processor's hardware is not capable of executing all the instructions in the pipeline simultaneously.
- Structural Hazards within a single pipeline are rare on modern processors because the instructions Set Architecture is designed to support pipelining.
- **Data Hazards:** This hazard arises when an instruction depends on the result of a previous instruction, but this result is not available.
- These are divided into four categories.
  - RAW - Hazard
  - RAR - Hazard
  - WAW - Hazard
  - WAR – Hazard
- **RAR Hazard:** RAR Hazard occurs when two instructions both from the same register. This hazard does not came from problem for the processor because reading a register does not change the register's value. Therefore, two instructions that have RAR Hazard can execute on successive cycles.
- **RAW Hazard:** This hazard occurs when an instruction reads a register that was written by a previous instruction. These are called as data dependencies.
- **WAR and WAW** are also called as name dependencies.

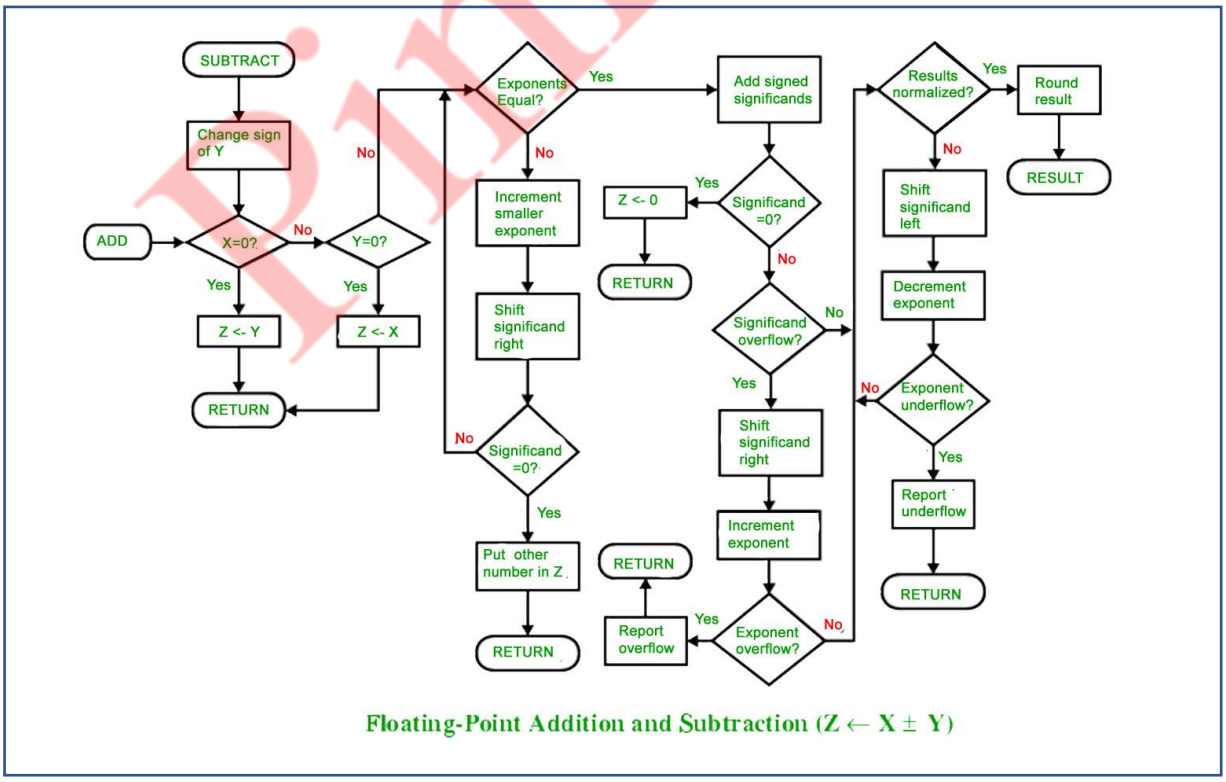
- These hazards occurs when the output register of an instruction has been either read or written by a previous instruction.
- If the processor executes instructions in the order that they appear in the program and uses the same pipeline for the instructions, WAR and WAW hazards do not cause any problem in execution process.
- **Branch Hazards:** Branch instructions, particularly conditional branch instructions, create data dependencies between the branch instruction and the previous instruction, fetch stage of the pipeline.
- Since the branch instruction computes the address of the next instruction that the instruction fetch stage should fetch from, it consumes some time and also some time is required to flush the pipeline and fetch instructions from target location. This time wasted is called as branch penalty.

---

b) Draw and explain floating point addition and subtraction algorithm. (10 M)

Ans:

- In floating point arithmetic, addition and subtraction are more complex than multiplication and division. Addition and subtraction operations are carried out in four basic phases.
    - Check for zeros
    - Align the significant
    - Add or subtract the significant
    - Normalize the result



Floating-Point Addition and Subtraction ($Z \leftarrow X \pm Y$)

- In the next phase, exponents of the two numbers X and Y are made equal. Alignment is achieved by shifting either the smaller number to its right or shifting the larger number to the left.
- Since either operation may result is loss of digits, it is the smaller number is shifted. The alignment is achieved by repeatedly shifting the magnitude portion of the significant right 1 digit and incrementing the exponent until the two digit exponents are equal.
- Next, the two significant are added together, taking into account their signs. Since the sign may differ, the result may be 0. There is also the possibility of significant overflow.
- Next, result Is normalized. Normalisation consists of significant digits left until the most significant digits is nonzero. Each shift causes a decrement of the exponent and thus could cause an exponent overflow.
